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SAR++: A Multi-Channel Scalable and Reconfigurable SAR System

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***Abstract*– SAR++ is a technology program aiming at developing know-how and technology needed to design the next generation civilian SAR systems. Technology has reached a state, which allows major parts of the digital subsystem to be built using custom-off-the-shelf (COTS) components. A design goal is to design a modular, scalable and reconfigurable SAR system using such components, in order to ensure maximum flexibility for the users of the actual system and for future system updates. Having these aspects in mind the SAR++ system is presented with focus on the digital subsystem architecture and the analog to digital interface.**

I. INTRODUCTION

The Danish SAR program has developed and operated EMISAR, a dual-frequency, fully polarimetric and interferometric, SAR system since 1995. EMISAR was designed for the triple purpose of 1) obtaining experience with SAR design, 2) acquiring data for remote-sensing research, and 3) being a research vehicle for SAR system research. EMISAR was designed to be reconfigurable within the limitations of the technology available at the time of development. The performance of this system is briefly presented with emphasis on the aspect of reconfigurability.

The concept of reconfiguration can be viewed in three perspectives of which the first two melts together for a satellite borne unit. 1) A reconfigurable and scalable design has the potential of optimum price/performance at the time of construction. 2) Before each mission, it is possible to choose the optimum load for a given set of tasks and it may be feasible to replace some units with newer ones thus taking advantage of the steady improvement of modern electronics. 3) During a mission a reconfigurable system may permit trade-offs between e.g. resolution, swath, number of polarization channels, number of frequencies, maximum range etc. thus enabling the choice of optimum parameters for a specific task.

Examples of the type 3 configuration perspectives are given in section II, where reconfigurability aspects of the EMISAR system, which currently is being operated, is described. Type 1-2 configuration(s) are currently investigated in the ongoing technology program called SAR++, see section III and IV. Here are also presented possible components, which could apply for the SAR++ digital architecture. The principle of using custom-off-the-shelf (COTS) components instead of dedicated modules along with the importance of using standardized modules are also explained. Using COTS technology makes it feasible to take advantage of the progress in commercial equipment particularly obvious in the computer and data communication areas.

The major part of digital hardware of the SAR++ system can be build using COTS components at board / subsystems complexity. However for the analog to digital interface, needed in the receive path, no components which fullfills all system requirements seems to be available. Components at IC / ASIC level can be found. An example of such a dedicated board design is described in section IV.

II. EMISAR

The old EMISAR [1] system supports dual frequency (L- and C-band), polarimetry and across track inferometry (XTI). The system is equipped with one 3-axes stabilized antenna and two flush mounted (non-steerable) XTI antennas (C-band) vertically spaced by 1.14 meter. The two receivers supports 4 channels simultaneously, 2 frequencies combined with 2 polarizations.

The system bandwidth can be reduced, at the costs of a coarser range resolution, and this enables the data rate to be reduced accordingly. The range pre-filter, which takes care of the decimation, is located in front of an 8192 samples buffer in the receiver. Reducing the data rate before the buffer allows the slant swath width to be increased. The azimuth pre-filter can be used to reduce the data rate in the receiver. The decimation rate of the azimuth pre-filter is typical 4 for the steerable antenna and 1 for the other antennas (@ 2 m resolution). The azimuth pre-filter option cannot be used in combination with the XTI antennas, because the filter is a low pass filter and zero Doppler shift cannot be expected from the flush mounted antennas.

Reconfiguring the mentioned parameters allows for many combinations of range resolution, slant swath width and the number of channels / polarizations received. Some of these configurations are shown for one of the two receivers in Table 1. Not all combinations are valid, when two antennas are chosen the total data rate must not exceed the maximum performance of the storage system (30Mbyte/s).

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TABLE 1.
CONFIGURATION EXAMPLES FOR THE TWO XTI ANTENNAS.

	Range Resolution	*Slant swath*	*Data rate in % of maximum tape drive capacity*
Polarimetri (quad pol)	2 m	4.5 km	66.7 %
Polarimetri (quad pol)	2 m	6 km	88.9 %
Polarimetri (quad pol)	4 m	6 km	44.4 %
Polarimetri (quad pol)	4 m	9 km	66.7 %
Polarimetri (quad pol)	4 m	12 km	89.9 %
Dual baselines XTI	2 m	4.5 km	66.7 %
Dual baselines XTI	2 m	6 km	88.9 %
Single baseline XTI	2 m	6 km	44.4 %
Single baseline XTI	2 m	9 km	66.7 %
VV or HH (single pol)	2 m	6 km	22.2 %
VV or HH (single pol)	2 m	9 km	33.3 %
VV or HH (single pol)	2 m	12 km	44.4 %

III. SAR++

A technology program denoted SAR++ is ongoing at DTU aiming at developing the technologies and know-how needed to design the next generation civilian SAR systems. The design goal is a multi-frequency, polarimetric, SAR system with a bandwidth of up to 800 MHz depending on carrier frequency and thus achievable antenna bandwidth and frequency restrictions.

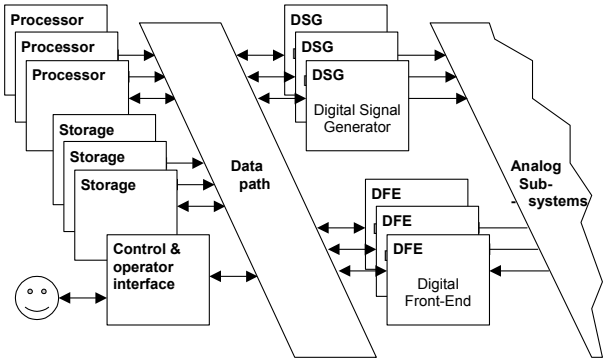

Fig. 1: SAR++ Digital Subsystems Overview

Fig. 1 shows the overview of the digital subsystem. Note that the illustration above implies an architectural structure which closely resembles that of a high performance computer with a set of interfaces (I/O) connecting the analog subsystems. An important feature is the data path, which is build as a scalable network (Myrinet, [13]) allowing the system to be expanded without having a performance bottleneck in the data path.

Referring to Fig. 1, the processors in the top left corner could be implemented using distributed computers from CSPI, [2], or equivalent. CSPI provides a 6U-sized board which contains 4 x 400 MHz, Altivec PowerPC, and an onboard Myrinet 2000 switch allowing a compact real time processor (RTP) to be implemented. The software aspect of this RTP is probably more important than the hardware as the software can be expected to have longer lifetime than the hardware. Software components as operating systems Linux / vxWorks and standardized libraries MPI, [3], and VISPL, [4], are likely to be upgraded to newer / future hardware enabling the hardware of the RTP to be upgraded with minimum design effort. At the same time the use of common software provides a large selection of system development and debug tools easing the software development.

Since the class of algorithms to be run on the RTP is known, it is possible to optimize the balance between the network and CPU performance of the RTP as shown in [5].

The control computer performs a vide range of tasks which typically does not require much performance of the host computer. Examples are logging of aircraft navigation data via a 1553 interface, control of the aircraft flight direction, and setting up parameters for each scene to be mapped, as described in section II. The hardware components can be a CompactPCI system, including a single board computer, various I/O cards e.g. for controlling the settings of the analog subsystem. Many of the comments on the software for the RTP also apply for the software on the control computer.

Experience has shown that the operator / user interface should be networked and platform independent allowing great flexibility during design, test and operation. The operator console may be a commodity laptop PC running X-windows or a web based JAVA client.

The storage system of Fig. 1 can be implemented using disk and/or tape arrays. The storage bandwidth for the SAR++ system may be as high as 400 Mbyte/s equals 1.4 Tbyte/hour [6]. The tape drives for the computing backup marked are possible candidates. Several examples of drives with a sustained data rate of approximately 16 Mbyte/s and a storage capacity of 100 Gbyte exist [7]. Hard disk drives has a sustained data rate, which is 2-3 times higher, see [8] and [9]. Tape drives has the advantage of the exchangeable media, which enables the high storage capacity needed for large area mapping. Hard disks has the advantage over tape drives of being cheaper and more compact for the same data rate, which makes disks suitable for relative small scenes (approx. one hour of acquisition pr. mission).

IV. ANALOG TO DIGITAL INTERFACE

A Digital Front End (DFE) board is currently under development. The DFE include two A/D converters, each sampling at 1 GHz. The two inputs enable the DFE to support both analog and digital demodulation (800 MHz. analog bandwidth). In both cases the two converters needs to be synchronized and in the latter case the two converters are operated to emulate one 2 GHz converter [10].

An FPGA is included for control of the data flow (data framing) and to perform initial signal processing (Digital demodulation, decimating filters) [11].

A buffer is needed to smooth the incoming data-bursts of 2Gsamples/second to the average outgoing data rate of 400 Mbyte/s [6]. The buffer size needed is one burst-length, which is 64K complex data samples or 128KByte. High density FPGAs may support this, but there are several advantages of including a larger buffer. Fast DDR SRAM designed for the data and telecommunication marked are available for this purpose.

The interface from the DFE to the rest of the digital system can be designed in different ways of which two are discussed: 1) Direct memory access (DMA) and 2) a direct network interface. In the DMA case the DFE could be designed as a cPCI board where the buffer memory is mapped to the PCI address space. Radar data could be transferred via the PCI bus to a network interface or a storage interface e.g. a SCSI LVDS bus or Fibre Channel interface. Such interfaces often require large size messages (0.5 Mbyte) in order to approach their maximum data transfer rate [12]. Consequently the DFE board must have a large buffer to support these large messages and to ensure flexibility in the choice of e.g. storage interfaces.

A drawback of the DMA type solution is that a local control computer is needed at the analog to digital interface (size / electrical noise problems). This control computer can be avoided using a direct network type of interface. In this case the data are sent directly via a network to either a real time processor (distributed network coupled computers) or a centralized control computer.

A single network interface supporting the 400 Mbyte/s data rate needed at the SAR++ DFE network interface may not be optimal from a practical COTS design viewpoint. Multiple network channels may be economically more feasible in the sense that a number of thin channels may be cheaper than one wide/fast channel. It is also easier to (down) scale the network interface for a given application, which does not require 400 Mbyte/s output data rate. A DFE buffer supporting several data bursts has the advantage over a small buffer that a burst does not need to be segmented into smaller packages in case of multiple output channels. If the radar data are sent to a multi-processor entity, it is an advantage for the succeeding signal processing, if each processor receives a full range line and not only a part of a range line.

COTS networks are available: e.g. Myrinet [13] and RapidIO [14]. Myrinet has a relatively simple electrical interface and a relative simple routing / data packet format which is feasible for FPGA implementation. The GM protocol stack, supplied with Myrinet, has a so called raw interface which enables the data to be received using a normal Myrinet interface card. The RapidIO interface is designed for embedded systems and promises FPGA interfaces using only a small part of the available logic.

All in all the proposed DFE, which can be build using COTS components (ICs), is very flexible and can be reconfigured by reprogramming the FPGA. This allows the DFE to be used in many different radar systems with bandwidth requirements up to 800 MHz. The prototype DFE PCB area will be 10cm x 16cm, the major components are two ADCs, one FPGA and one SRAM.

VI. CONCLUSIONS

Different aspects of scalable and reconfigurable SAR systems are presented and discussed using an old and a new SAR system as examples. For the old EMISAR system, it is shown how this system can be reconfigured via a number of parameters. The SAR++ system is presented with focus on the digital subsystem architecture and the analog to digital interface.

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